Design Vedic Multiplier Using Reversible Gates

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Abstract - In modern times reversible logic fascinate attention to produce something better in certain fields like nanotechnology, quantum computing and low power design. Along with high speed multiplier architecture becomes need of the day as multiplier unit forms an integral part of processor design. Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculations. In this paper we introduce a novel architecture of 4-bit reversible vedic Multiplier is represented which is based on vedic mathematics and reversible logic. In proposed design we try to optimize path delay & memory usage compared to conventional Vedic multiplier.

Index Terms— ancient, fascinate, nanotechnology, quantum.

1 INTRODUCTION

TODAY two different ancient methods are available to do large and complex calculations in head without need of any modern day electronic devices. These techniques are: 1) Abacus Math & 2) Vedic Math. Abacus is used as a tool to learn calculations while Vedic Mathematics has no legal definition. Hindu philosophy is based on Vedas and mathematics translated from these texts is termed as Vedic Mathematics. The system is based on 16 Vedic sutras or aphorisms, which are actually word-formulae describing natural ways of solving a whole range of mathematical problems.

On other hand Reversible logic is gaining interest in the recent past due to its less heat dissipating characteristics. All quantum computations are necessarily reversible. Therefore, research of reversible logic is beneficial to the development of future quantum technologies. Recently, several researchers have focused their work on the design and synthesis of efficient reversible logic circuits. In the design of reversible logic circuits the following points must be considered to achieve an optimized circuit. They are:-

- Fan-out is not permitted.
- Loops or feedbacks are not permitted.
- Garbage outputs must be minimum.
- Minimum delay.

2 Vedic Sutras

The Sanskrit word Veda is derived from the root "Vid" which means to know without limit. The word Veda covers all Veda-shakhas known to humanity. The Veda is a repository of all knowledge, fathomless, ever revealing as it is delved deeper. Swami Bharati Krishna Tirtha (1884-1960), former Jagadguru Shankaracharya of Puri, gather a set of 16 Sutras and 13 Sub – Sutras from the Atharva Veda. He developed methods and skill for large principles contained in the aphorisms and their corollaries, and called it Vedic Mathematics. According to him, there has been considerable literature on Mathematics in the Veda-shakhas. There are 1131 Veda-shakhas but today only about ten Veda-shakhas are presently in the knowledge of the Vedic scholars in the country.[2]

Urdhva- triyakbhyam Sutra

The formula simply means: "Vertically and crosswise"

Urdhva – Tiryagbhyam sutra is a general multiplication formula applicable to all cases of multiplication. The digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and hence the process goes on. If more than one line are there in one step, all the results are added to the previous carry. In each step, least significant bit acts as the result bit and all other bits act as carry for the next step. Initially the carry is taken to be zero.

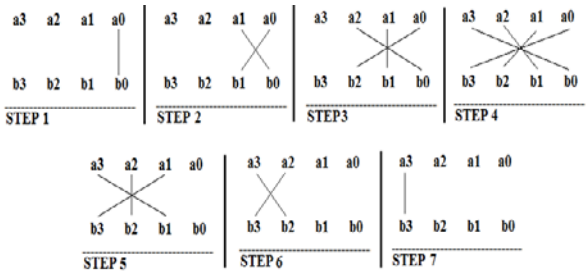

Figure 1: Graphical presentation of 4-bit multiplication using Urdhva-triyakbhyam Sutra.

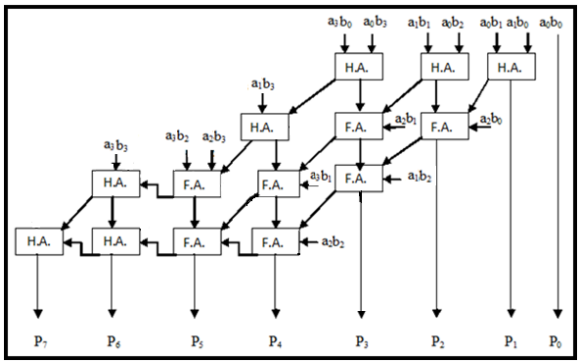

Figure 2: Conventional Architecture of Urdhva-triyakbhyam Sutra.

3 Reversible Logic

Reversible logic is very essential for the construction of low power, low loss computational structures which are very essential for the construction of arithmetic circuits used in quantum computation, nanotechnology and other low power digital circuits. It has been proved that any Boolean function can be implemented using reversible gates. Higher levels of integration and new fabrication processes have dramatically reduced the heat loss over the last decades. The power dissipation in a circuit can be reduced by the use of Reversible logic. An Irreversible circuit dissipates energy due to information loss. Landauer's principles state clearly that, there is a minimum possible amount of energy required to change one bit of information known as Landauer limit:

$$E = kT\ln 2$$

Where,

E→ Energy of 1-bit information

K → Boltzmann constant (1.38×10^{-23} J/K)

T → Temperature

ln2→ natural log of 2 (0.69315)

At room temperature (25°c or 298.15 K), the Landauer limit represents an energy of approximately 0.0178 eV or 2.85 zJ.[3][4]

4 Proposed Design

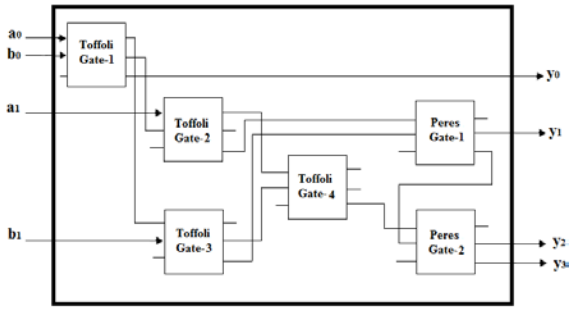

Fig.3: Reversible 2X2 Vedic multiplier

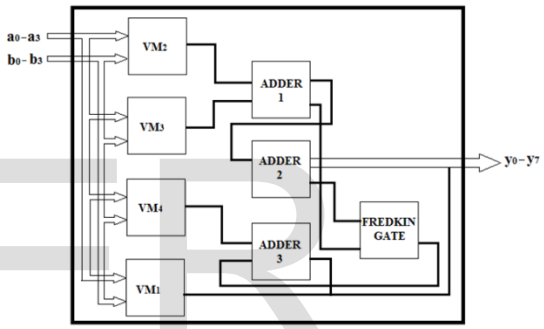

Fig.4: Reversible 4X4 Vedic multiplier

5 Result

To verify comparison first we have run program for conventional Urdhvatriyakbhyam Vedic Multiplier (UTVM) which is based on half adder and full adder. The focus of work centered on reversible Urdhvatriyakbhyam Vedic Multiplier for minimizing path delay and memory size.

Schematic

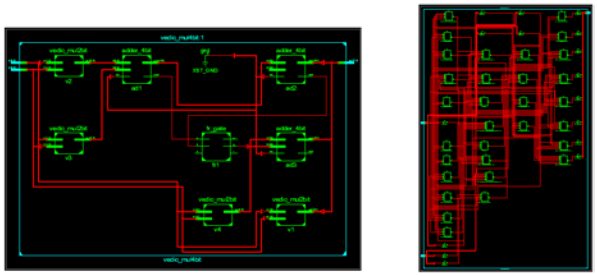

Fig.5: RTL Schematic And Technology Schematic for Reversible (4x4)-bit Vedic Multiplier

Output

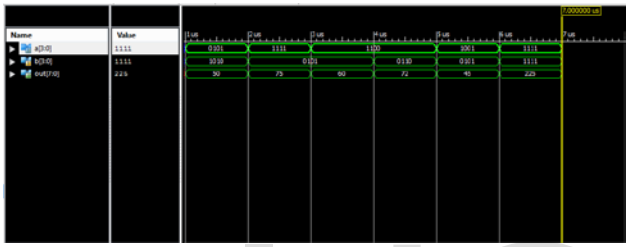

Fig.6: Result for Reversible (4x4)-bit Vedic Multiplier

Table.1: 4-bit multiplication summary

Method	Maximum combinational path delay	Total memory usage
Conventional UTVM	13.459ns	259372 kilobytes
Reversible UTVM	11.289ns	231936 kilobytes

6 Conclusion

Reversible logic has proven itself the modern way of digital logic circuit designing. Here in this paper we have designed reversible circuits for Urdhvatriyakbhyam Vedic Multiplier which is logically verified using XILINX 14.2. The simulation results and device summary are as shown in figures 5) and 6) respectively. The proposed circuits with reversible gate is proven advantageous than conventional circuits and it will help the researchers in low power logical design applications.

7 References

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